New Approach to Class B Amplifier Design

by Peter Blomley*

(Concluded from February issue)

This article describes a 30-watt amplifier design which embodies the author's approach to class B design, outlined last issue. Although further work on this approach is still needed, the design illustrates the kind of problems involved. The author also discusses the application of integrated components in future designs.

The general design of a complete amplifier using the new approach is relatively conventional except for the inclusion of the signal splitter (described last month). In principle, the design of each half of the output stage is made simpler as there is no cut-off, hence removing the necessity for predicting the performance in the cross-over region.

Examination of the circuit (Fig. 1) shows that the amplifier consists of three sections, the input amplifier, signal splitter and output amplifier.

Input amplifier. This converts the input voltage into a proportional output current which drives the signal splitter. To enhance the performance of the amplifier as a whole, this section should have a reasonable mutual conductance (1A/V) and good linearity (1%). The latter does not represent a serious problem as the input amplifier is a low-level class A amplifier, but care is needed to control the maximum value of g_m otherwise frequency compensation problems arise.

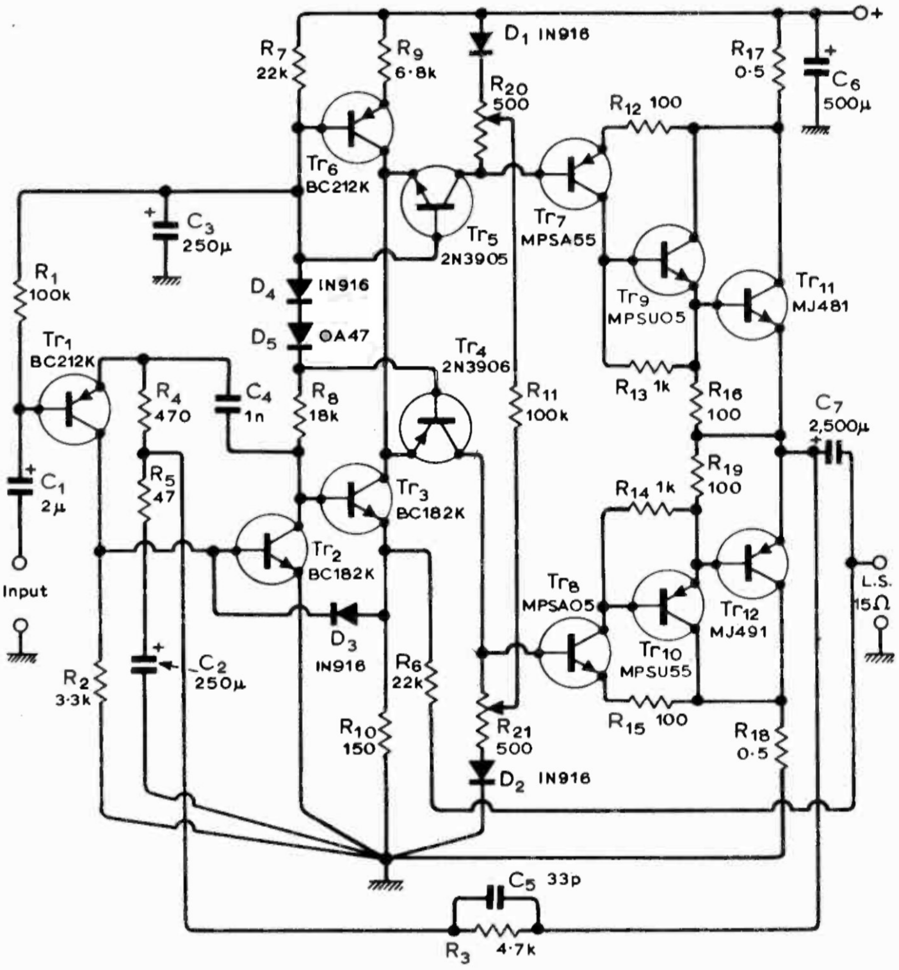

Fig. 1. Complete power amplifier circuit using new approach. Design gives harmonic distortion of 0.01% at all power levels and intermodulation distortion of 0.003%.

Signal splitter. As many fundamental details of the signal splitter were described last month, further details are confined to the biasing system. If perfect bipolar devices were available and ideal current sources existed, voltage bias across the emitter-base junction would not be needed, but such situations do not exist and distortions due to conditions falling short of the ideal can be rendered negligible by employing simple bias diodes (Fig. 2). This reduces the voltage excursion at the input to the signal splitter from 1.2V to 300mV pk-pk. The waveform with a sinusoidal output current is shown in Fig. 3.

Output stages. This now is one of the easiest to design. As long as the gain remains constant throughout the output cycle all is well. In the initial version, used to evaluate system performance, a compromise was reached between complexity, performance and cost. Thus individual adjustment potentiometers were used instead of the matched devices.

The output sub-amplifiers are similar to the Quad triples, these giving excellent linearity down to very low output currents, coupled with outstanding thermal stability. To compensate for the effect of ambient temperature changes on the quiescent current of the amplifier, diodes D_1 and D_2 cancel V_{BE} changes in transistors Tr_7 and Tr_8. It may have occurred to the reader that diodes in the forward path of the amplifier loop could generate appreciable distortion. However, in practice the maximum change in current is about 4:1 and thus almost corresponds to the change in collector current of transistors Tr_7 and Tr_8. In this way the change in voltage drop across the transistors compensates for the change in the diodes. Even if this did not occur, the resultant gain change for the output sub-amplifier is less than 4% for I_{out} values between 0 and 2A. The problem can be alleviated by increasing the current into

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diodes D_1 and D_2 and adding one resistor, but the advantages gained from this are negligible.

Circuit description

The function of Tr_1, Tr_2, and Tr_3 is to convert an error voltage—the difference between the input and feedback voltage—into a proportional output current. Now to produce the required mutual conductance of this stage (1A/V) without sacrificing either noise performance or linearity, the design in Fig. 1 was used. Starting at the input transistor Tr_1, this p-n-p type is used mainly as a level shifter. If we assume that the current gain of Tr_2 was extremely large (> 500), then this input stage would have a maximum voltage gain of about five—not very much! If voltage gain was increased to the theoretical maximum of 30 (by decreasing the value of R_2 and R_4) problems would arise with the voltage offset at the speaker output due to increased emitter current flowing through R_3 and base current flowing through R_1.

Assuming for the moment that this first stage gain is a reasonable compromise, it now becomes obvious that the noise and distortion performance is dictated by the next stage. This stage (Tr_2, R_8) is a straightforward class A amplifier with very high gain (typically 400) and low distortion due to the limited modulation index of the collector current (0.04 max). The peak 2nd harmonic voltage generated is about 10μV and, assuming this is referred to the input of the first stage, it represents less than 0.001% 2nd harmonic distortion with feedback. Thus this second stage is the work horse of the input section, the third device Tr_3 being used both as a buffer to reduce the loading of R_{10} on R_8, and to convert the voltage changes across R_8 into an output current to drive the emitters of the signal splitter.

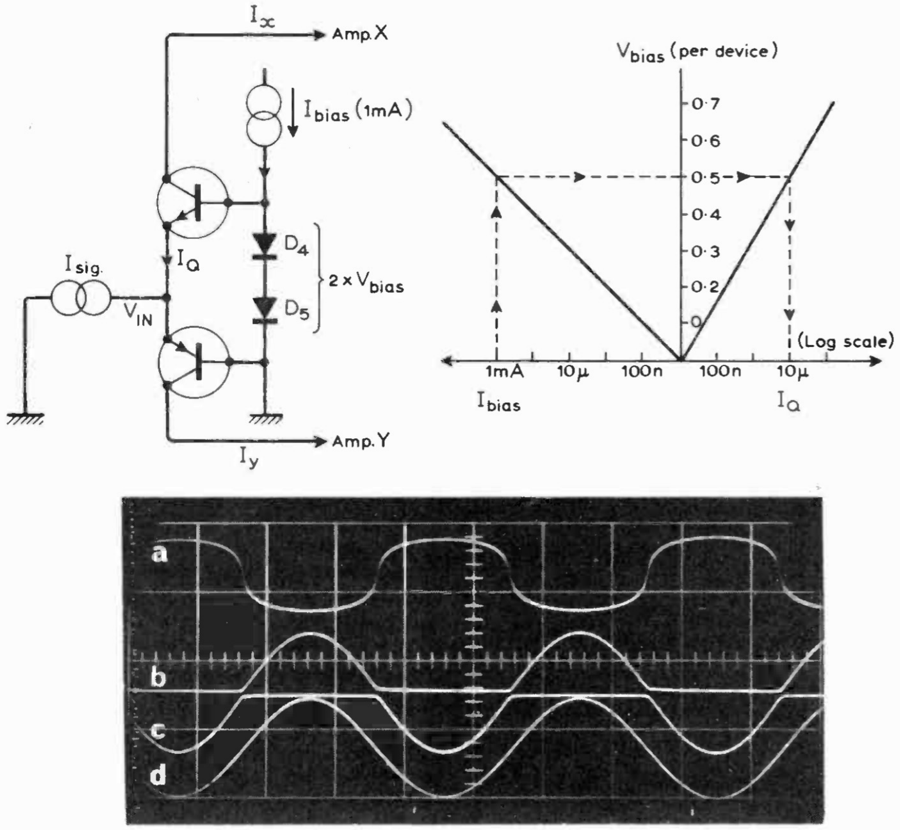
Resistor R_{10} performs two functions in this last stage of the input section. It defines the conversion constant *Engmen* for the stage, and it governs the maximum current which can be driven out of the collector of Tr_3. (This maximum current is defined by using the conducting voltages of D_3 and Tr_2 and the value of R_{10}.) Therefore this input section seems to have excellent performance during normal operation, but what can happen during an overload?

If the input transient was negative all would be well due to Tr_2 entering saturation. But if the transient was positive Tr_1 would turn off completely, the potential across R_{10} rising toward that at the end of R_8. (Tr_2 would also be completely cut off.) This would cause excess currents to flow in Tr_3, upsetting the bias chain R_7, D_4, D_5, R_8. After the excessive input signal is removed some time would elapse before recovery would take place, hence diode D_3 clamps the voltage and maintains Tr_2 in full conduction to reduce recovery time and improve amplifier stability.

While discussing the problem of recovery from overload, the charge across the compensation capacitor C_4 has also to be taken into account. The time for the accumulated charge to decay is a function of the amount of charge and the rate of decay. If the rate of decay is constant, the only way to reduce the recovery time is to limit the accumulated charge (in terms of voltage). Diode D_3 performs this function as well as clamping the voltage across R_{10} at 1V thus limiting drive current into the signal splitter.

The second section is the signal splitter, unique to this approach, and consists of transistors Tr_4 and Tr_5 plus a current source transistor Tr_6. The signal current into the emitter of Tr_4 or Tr_5 is derived by subtraction of two current levels, one constant and set by the voltage across R_9, and the other the output current of the input section. This signal current either appears at the collector of Tr_5—causing a voltage change across R_{20}—or at the collector of Tr_4—causing a voltage change across R_{21}. These voltage changes are converted into positive and negative output currents in the output section, which are then added together to give the final waveform. The current gain of the output sections which are conventional triples are governed by the ratio of R_{20} to R_{17} and R_{21} to R_{18}, and in this case the gain of 1000 seemed reasonable.

To keep the output triples above the minimum conduction level a bias current is provided by R_{11}. The procedure adopted for setting the standing current is to first set R_{20} and R_{21} to minimum (diode end).



Curve a – Emitter voltage 200mV/cm
" b – I_y collector current 1mA/cm
" c – Collector current 1mA/cm
" d – I_{sig} 1mA/cm
Vertical and horizontal scales = 0·2 millisec/cm Frequency = 1kHz

Fig. 2. Input amplifier converts signal voltage to a proportional current to feed transistor signal splitter. Bias diodes reduce voltage excursion from 1.2V to 300mV pk-pk. Bottom trace is current signal input to splitter.

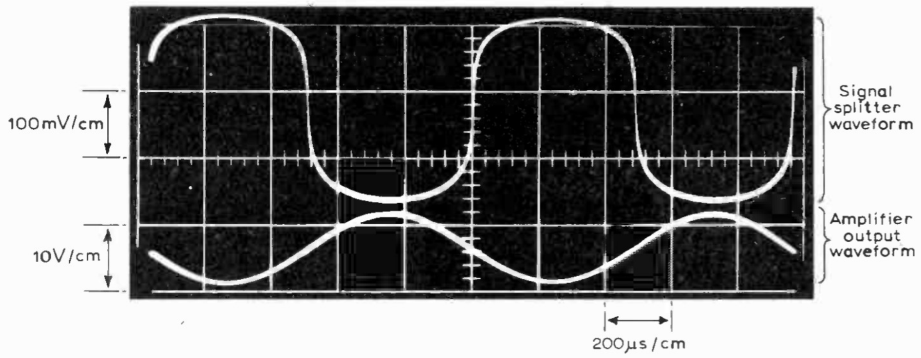


Fig. 3. Voltage excursion at signal splitter input with corresponding sinusoidal amplifier output current ($R_L = 15\Omega$).

Set quiescent current with R_{20} and increase R_{21} until there is a small increase in current.

The only part still to be described is the biasing chain R_7-D_4-D_5-R_8-C_3. This provides the half supply voltage for the base of Tr_1 (decoupled by C_3), a load for the class A stage Tr_2, and sets devices Tr_4 and Tr_5 at the minimum conduction level required for good phase response during cross-over —by using the voltage across D_1 and D_2. By increasing the value of C_3 it is possible to reduce the rate of charging of the speaker coupling capacitor, eliminating 'thump', but capacitor size becomes very large.

Returning for a moment to the input section, Tr_2 is in a similar position to that used in many amplifiers, but instead of driving another stage (Tr_3) which only requires a limited voltage swing, it is the prime mover for the output section. To have sufficient drive capability the quiescent current in this stage may well need to be 10mA—instead of the 1mA in mine—and the voltage swing on the collector will be the full supply voltage (50 volts).

It now seems clear why the distortion of many amplifiers rises at low frequencies. The dissipation change of this device during a voltage cycle could be 500mW pk-pk in the case I have quoted giving an emitter-base voltage change at low frequencies of about 100mV. This change, even if we assumed it is basically a linear function of voltage, will cause a non-linear change in the input device and hence a considerable rise in distortion at low frequencies. In my amplifier the maximum dissipation change in Tr_2 will be less than 1mW, thus eliminating this form of distortion and improving intermodulation performance.

Performance

The measurement of distortion created some difficulties especially when considering the range of frequencies over which this amplifier operates. The methods employed can be separated into two distinct techniques—spectrum analysis and nulling methods. To realize the first technique, an oscillator with a pure, single-line spectrum was needed, but the only one available at the time, approaching a reasonable performance, was the Si 451 produced by J. Sugden & Co, having a range up to 30kHz. This was found (excellent as it is) to be inadequate to permit the measurement of amplifier distortion.

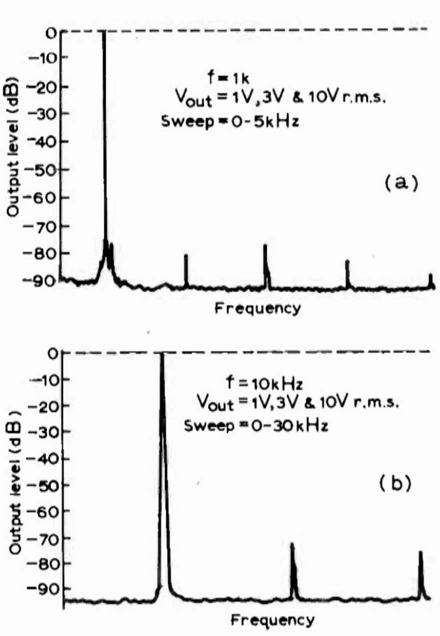


Fig. 4. Spectra made with a wave analyser showed no difference between spectra of outputs from oscillator and amplifier. Plots were made with (a) 1kHz and (b) 10kHz signals and were identical at all three power levels.

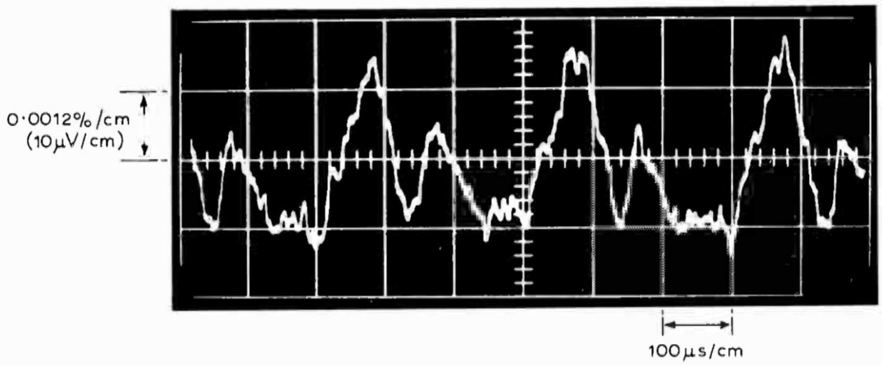


Fig. 5. Null method of assessing amplifier distortion shows distortion products to be well down in the noise. Deflection of 4cm represents 0.003% peak distortion at 10 watts (3kHz, 15Ω load).

So difficult in fact was the problem that it is impossible to publish distortion curves with any degree of confidence in their truth, but it can be said that using the Hewlett Packard 3590 wave analyser there was *no discernible difference* between a plot of the distortion of the oscillator and that taken after the oscillator output had been passed through the amplifier. Plots were taken over the frequency range 100Hz to 20kHz and powers of 100mW to 25W. As a matter of interest the spectrum plots of the amplifier are shown in Fig. 4 for 1kHz and 10kHz and at several power levels. The second method attempted was rather more successful but unfortunately does not present information in a usable form because it involves a comparison of output and input signals. It is also not a sequential test as in the previous method and as a result problems were encountered in successfully nulling the output against the input of the amplifier, due to the phasing of the signals and the earth loops generated by the measurement method. After considerable adjustment of the phase compensation and spurious pick-up difficulties the photograph Fig. 5 was obtained. Here the distortion generated is right in the noise (−120dB down from 20V r.m.s.) and the total deflection of 4cm represents 0.003% peak distortion at 10 watts and a frequency of 3kHz, chosen for easiest phase cancellation. The spikes usually evident in the difference waveform with this type of amplifier are completely absent, even with reactive loads, indicating that stability in the cross-over region must be excellent.

Intermodulation performance

The use of these two techniques is limited in one way or another to the evaluation of amplifier linearity. The main advantage is, of course, that a direct numerical value of distortion is obtained which can be used in comparison with other amplifiers.

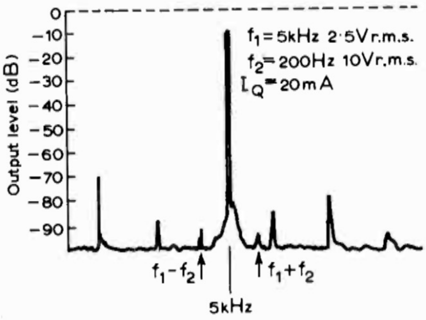


Fig. 6. Result of feeding 5kHz and 200Hz signals in a 16:1 power ratio into amplifier. Intermodulation products f_1+f_2 and f_1-f_2 are 90dB below 200 Hz signal. Other spectral lines are due to generator distortion.

The intermodulation test does not rely on low-distortion oscillators of signal cancelling techniques—in fact the only component which limits the measurement accuracy is the wave analyser itself. The real drawback is seen when an interpretation of the results is necessary! The method adopted is to "sweep" the transfer characteristic of the amplifier with a low-frequency signal of large amplitude, and to "measure" the slope of the characteristic with a low-level high-frequency signal. The two frequencies selected were 200Hz and 5kHz in a power ratio of 16:1.

The results not only ease the assessment of the amplifier performance in an absolute sense but also give some form of subjective measurement for comparison with other elements in the system. The results obtained in Fig. 6 indicate an excellent performance, the intermodulation products $f_1 + f_2$ and $f_1 - f_2$ are −90dB below the sweeping signal (200Hz) all other spectral lines being due to generator distortion.

Amplitude-frequency response

The type of frequency compensation used for this amplifier is unusual, mainly as a result of the system design. The open-loop gain begins to fall off at about 4kHz and continues on a 6dB/octave roll-off to about

500kHz where the second pole of the output section starts to contribute excess phase shift. The choice of the position of the dominant compensation was a difficult one. If it was placed in the output section, as is normally the case, the gain of the input amplifier would have to be restricted at low frequencies, affecting the distortion performance of the amplifier.

Another choice was using the dominant lag to encompass the output section as well as part of the input amplifier. This would lead to instability internal to the loop enclosed by the dominant lag and thus an internal pole would have to be introduced to remedy this condition. The final choice (shown in Fig. 7) gives the single-pole compensation needed for unconditional stability coupled with minimal high-frequency distortion. The inherent pole in the output section is subdued by the feedback resistance R_3 (so far as the main loop is concerned) but gives the required unconditional stability of the output section.

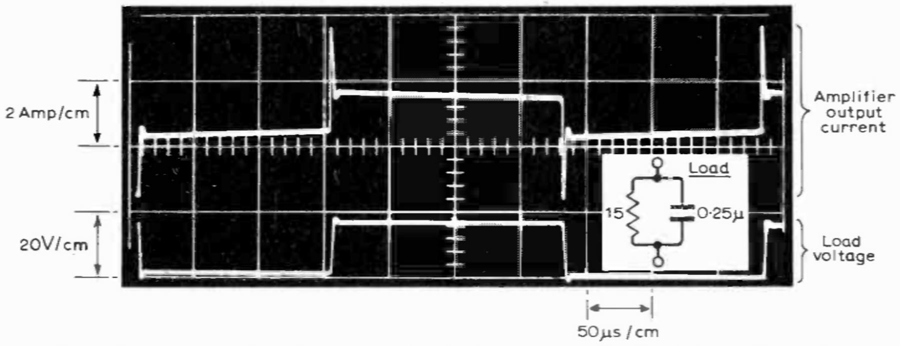


Fig. 9. Performance with a capacitative load. Capacitor in feedback loop effectively reduces maximum rate of change of voltage across load. Overshoot is much less when fed from a pre-amplifier.

Performance—with 60V regulated supply

output power	20 watts into 15 ohms 30 watts into 8 ohms
power response	30Hz to 100kHz (−3dB)
output impedance	0.1 ohm at 1kHz
total harmonic distortion	< 0.01% throughout audio band and all power levels
intermodulate distortion	< 0.003%
voltage gain	100
noise level	−120dB below full power
maximum peak output current	±3 amps, approx.

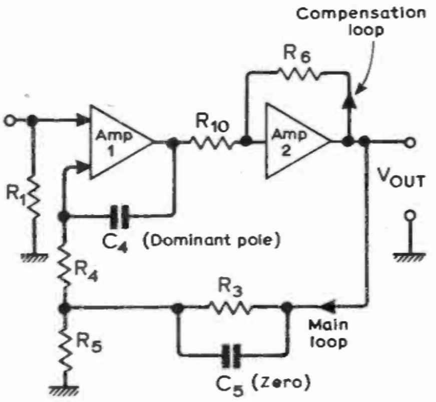
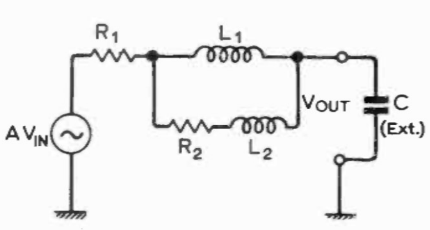


Fig. 7. Single-pole frequency compensation used gives unconditional stability coupled with minimal h.f. distortion.



$$R_1 = \frac{1}{g_{m1}}\left(1 + \exp\left(K.\frac{I_{OUT}}{I_{MAX}}\right)\right)$$

$$L_1 = \frac{1}{2\pi f_2\ g_{m1}}$$

$$L_2 = \frac{1}{2\pi f_3\ g_{m2}}$$

$$R_2 = \frac{1}{g_{m2}}$$

Fig. 8. Power amplifier equivalent circuit. Simple analysis shows output impedance is controlled by main feedback loop, but in practice R_6 generates another loop effectively placing a damping resistance across the apparent output inductance.

The performance with reactive loads will be spoilt if the output impedance of the amplifier is controlled by the overall feedback loop, i.e

$$Z_{out} = \left(1 + j\frac{f_1}{f_2}\right) \Big/ g_m$$

where f_1 is the signal frequency and f_2 the open-loop −3dB frequency. This expression has a simple analogy with a series inductance and resistance, where $R = 1/g_m$ and $L = 1/2\,\pi\,g_m\,f_2$.

A little more work† shows that if a capacitive load is used the amplifier would have a response given by

$$G = \frac{1}{p^2T^2 + \alpha\,pT + 1}$$

This is the equation of a second-order system, where $\alpha\ (1/g_m) \sqrt{(C/L)}$, and the natural frequency of oscillation is $w_o = 1/T = 1/\sqrt{(LC)}$. If the amplifier has an overshoot it must be due to the overall amplifier having an α-value approaching zero. If we now assume typical values and examine the worst case condition, g_m = 10A/V, f_2 = 4kHz and $\alpha = 0.1$ (20dB peak), then $C = 4\mu F$ and w_o = 250kHz.

If this was a perfect model for the amplifier the overshoot would be excessive, but in practice the output impedance is not only a function of frequency but also of output current. Thus α gets larger (less overshoot) as the output current increases. The basic assumption of this simple analysis is that the output impedance is controlled by the main feedback loop, but in this amplifier resistor R_6 generates another loop which effectively places a damping resistance across the apparent output inductance (Fig. 8).

The only remaining improvement to the transient performance of the amplifier is by pole-zero cancellation using the feedback element. If this term seems somewhat academic, an alternative is to study the overshoot with a second-order system with various inputs. If the input is an ideal step the amplifier will give theoretical overshoots, but if the rate of rise of the input waveform is *decreased* the overshoot will reduce and eventually disappear. The capacitor (a zero) in the feedback loop is really reducing the maximum rate of change of the voltage across the load and hence the degree of excitation given to this inherently oscillatory system. By using this type of compensation excellent performance with reactive loads has been finally achieved (Fig. 9). The overshoot with capacitative loads, such as 4µF, is about 50% with an ideal step input and far less when fed via a preamplifier, thus no difficulties should be experienced with any normal load.

Electrostatic loads. The distortion characteristic with this type of load was still insignificant below 10kHz and gave a gradual rise up to 20kHz where it was still less than 0.05% at maximum output‡. Square-wave performance is shown in Fig. 10 at maximum ‡output. The ringing is due to the finite output impedance converting the ringing current in the inductance and capacitance of the load into ripples in the output, plus the overshoot of the amplifier itself.

Future developments

The amplifier design is hopefully only a source of ideas which may encourage further research into the whole approach to design. So that the trend may be continued, future proposals are outlined in Fig. 11. Here, the main difference is that

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† See for instance "Active filters" F. E. J. Girling and E. F. Good, *Wireless World*, vol. 75, Sept. 1969, pp. 403-8.

‡ Maximum output is dictated by peak current output capability.

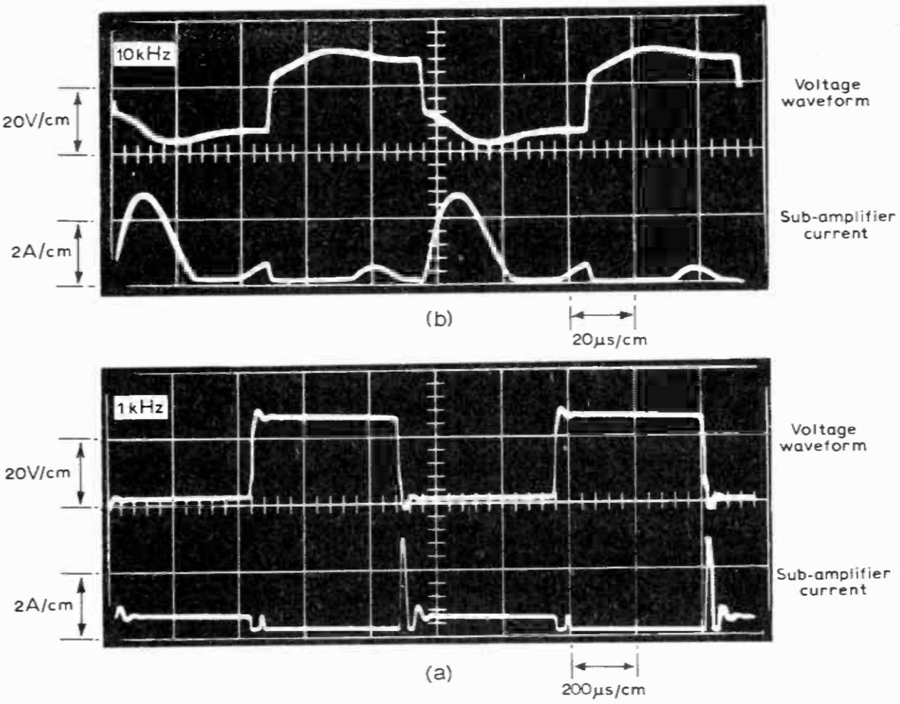

Fig. 10. Square-wave performance when driving electrostatic load at 1kHz (a) and 10kHz (b). Top traces are voltage and lower traces current out of sub-amplifier. Ringing is due to output impedance converting ringing current in L_2 and C_2 into ripples in the output.

the output subamplifiers are oriented toward the use of integrated components. It has become obvious that past problems with class B amplifiers originated with the stabilization of the quiescent current to give zero cross-over distortion. Attempts were made to use diodes to compensate for device V_{BE} changes with fluctuations in the *ambient* temperature—the independent variations due to device dissipation could not be eliminated. Most of the time the diode did its job and the voltage defined by the combination of transistor and diode remained constant. This constant voltage was used in conjunction with low-value resistors to set the quiescent current in the output circuits.

If now an integrated component is used both the diode and the transistor are on the same chip and, apart from minor fluctuations, the combination is isothermal. As a result the quiescent current is a function *only* of the setting voltage and not ambient temperature or differential device temperatures. The accuracy with which the current can be set is largely governed by the offset voltage of the transistor pair. Typical values of ± 4mV which would represent a ± 8mA inaccuracy in the quiescent current using 0.5-ohm feedback resistors are readily obtained. With such an arrangement a reasonable quiescent current for the sub-amplifiers would be 30mA, the worst case figures would be 24mA and 38mA. Both of these values are well above the low conductance current level (5mA) which is required for good linearity of the sub-amplifiers.

The advantage of the new approach is fairly evident when it is realized that as long as the amplifiers are above the non-linear region, the spreads introduced in the sub-amplifier quiescent current will not cause the class AB situation of over-biasing (shown last month) characteristic of present designs. It is now possible to design an output stage without the normal trim potentiometers, thus giving a degree of freedom in production not possible with current amplifiers. The performance of the amplifier, once checked at the end of a production line can be guaranteed for operation in any climate and for any period of time.

Possible applications

The performance of an amplifier of this calibre is, in my opinion, wasted in a conventional audio set-up. In most cases, the transducers will be the weakest link.

The approach used in the design of the output sub-amplifiers does not rely on complementary matched devices—in fact, in most cases n-p-n devices are preferred for their superior secondary breakdown characteristics. This represents considerable reduction in amplifier costs especially in the 100-watt region as presently available devices boast a V_{CEO} of 120V with 100 watts dissipation at a cost of less than 75p.

The ultimate use for this amplifier would appear to lie with the high-power professional market where the performance of cascaded amplifiers in a system would have to be excellent. Use in other fields would be mainly governed by the expected gain in performance or reduction in cost. A possible application would be as a portable standard oscillator, perhaps meter calibration amplifiers, or even high-frequency low-distortion class B transmitter amplifiers. However, these are only inspired guesses which may interest those working in these relevant fields.

Thanks are due to Peter J. Baxandall for his advice and encouragement and to Hewlett Packard and the Plessey Co. for use of their facilities.

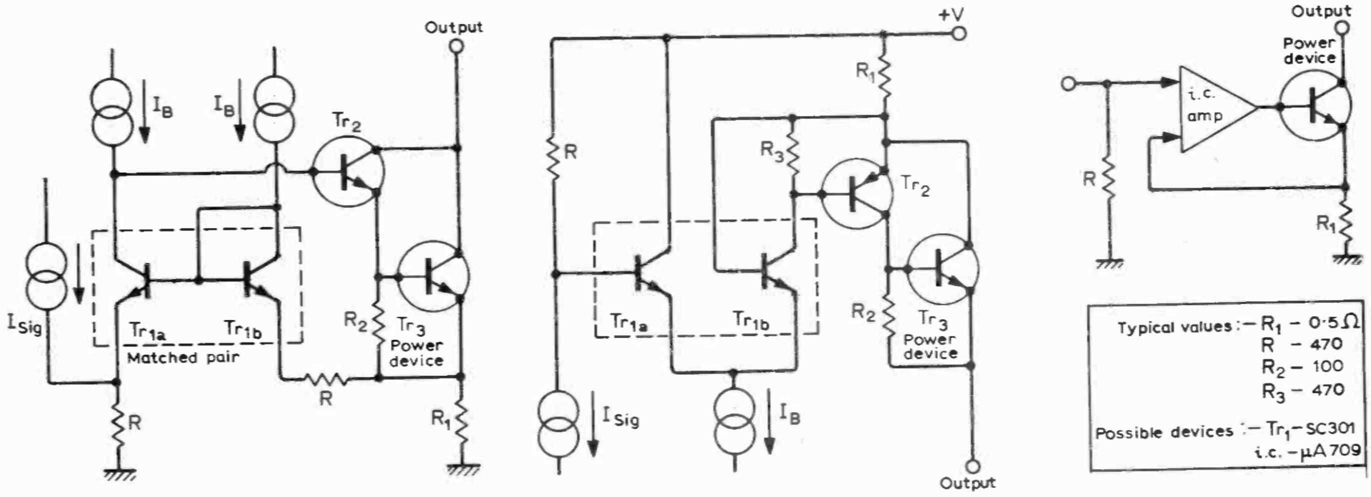

Fig. 11. Proposals for integrated components in output sub-amplifier.